## REMARKS

By this amendment, claims 1, 2, 8, 12, and 14 have been amended and claims 1-14 are active. This amendment is filed in reply to the outstanding Office Action of June 28, 2005, no new matter has been added and is believed to be fully responsive thereto and reconsideration is respectfully requested.

### Claim Objections

The Examiner objected to claims 1-11 because of certain informalities. The Examiner pointed out that the limitations in claim 1 concerning "of logic and memory" were enclosed in parenthesis and therefore such limitations did not carry patentable weight. This amendment removes the parenthesis used in claim 1 to overcome the Examiner's objection and ensure patentable weight to this limitation is taken into consideration.

### Rejection – 35 U.S.C. § 112

The Examiner rejected claims 1-13 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In particular, the Examiner indicated there was insufficient antecedent basis for the limitation "the logic scan chain results" in claims 1 and 12, "the logic tests" in claim 2, and "bypass mode" in claim 8. By this amendment the indefinite article "the" has been deleted in claims 1, 2, and 12. The Examiner should note that claim 8 depends on claim 7 which introduces the antecedent for bypass mode.

Based on the foregoing, it is respectfully submitted that the claims 1, 2, 8, and 12 should now be allowable under 35 U.S.C. § 112 second paragraph.

**Rejection – 35 U.S.C. § 103**

The Examiner rejected claims 1, 2 under 35 U.S.C. § 103(a) as being unpatentable in view of Kishi et al. (US597635) in view of Bhawmik (US5680543), and in further view of Clark (US6650589).

Regarding claim 1 the Examiner indicated that Kishi discloses a device with apparatus that is capable of simultaneously performing self-test on memory circuits and logic circuits including a memory BIST circuit. But actually Kishi teaches a method of where the test is performed when the memory is inactive (during time test) note Kishi Figure 2a. This does not require clock isolation as the clock in memory is inactive during a retention time test.

The Examiner also indicated that Kishi shows "bypass isolation elements" in Figure 6 (selectors 16 through 18). However these are not scan bypass elements, instead they switch the memory inputs between the mission mode source (15) and the BIST source (71).

The Examiner noted that Kishi does not disclose "a clocking including clocking isolation elements ...." but indicates that Bhawmik discloses a clock generator operating related frequencies associated with the scan chains. The Applicant noted that Kishi does not teach or suggest "clocking isolation " because his solution does not require it since his logic testing takes place at a time when there is no activity at the memory taking

advantage of the type of test being performed on the memory being a "a data holding test" requiring no clocking of the memory. Likewise Bhawmik is also solving a different problem and not using "clocking isolation elements" which permits in the present invention to clock the memory and the logic at independent frequencies. In fact Bhawmik teaches a technique where all scan chains are clocked at a given frequency and those scan chains which can not tolerate the magnitude of the frequency are disabled. This would prevent the present invention from testing simultaneously at two different frequencies. As such Kishi and Bhawmik are teaching away from our invention and it would be impossible to combine such references or to suggest the invention is obvious.

The Examiner suggests that Clark discloses voltage isolation elements, such as voltage regulator 60 that provides a single voltage to microprocessor core 20. The present invention uses the voltage isolation elements to isolate the voltage to chip contacts to allow the tester to set the voltage conditions to many separate values required for test rather than the single voltage taught by Clark. Claim 1 would not be obvious considering Kishmi in view of Bhawmik and in view of Clark under 35 U.S.C. § 103(a).

Furthermore, since Kishi does not teach scan bypass elements as discussed above he could not suggest a control line to control scan bypass elements contained in the dependant claims and since claims 2-11 all depend on claim 1 it is respectfully submitted that claims 2-11 should likewise be allowable under 35 U.S.C. § 103(a).

The Examiner rejected claims 12 and 13 under 35 U.S.C. § 103(a) as being unpatentable in view of Kishi et al. (US597635) in view of Clark (US6650589).

Regarding claim 12 the Examiner indicated that Kishi discloses a device with apparatus that is capable of simultaneously performing self-test on memory circuits and logic circuits including a memory BIST circuit. But actually Kishi teaches a method of where the test is performed when the memory is inactive (during time test) note Kishi Figure 2a. This does not require clock isolation as the clock in memory is inactive during a retention time test.

The Examiner also indicated that Kishi shows "bypass isolation elements" in Figure 6 (selectors 16 through 18). However these are not scan bypass elements, instead they switch the memory inputs between the mission mode source (15) and the BIST source (71).

The Examiner noted that Kishi does not disclose separating the logic and memory circuits using isolation elements, but suggested that Clark discloses voltage isolation elements, such as voltage regulator 60 that provides a single voltage to microprocessor core 20. The present invention uses the voltage isolation elements to isolate the voltage to chip contacts to allow the tester to set the voltage conditions to many separate values required for test rather than the single voltage taught by Clark. Further, Kishi does not teach or suggest scan chain isolation elements used for enabling or disabling BIST as explained above in connection with claim 1. Therefore, claim 12 could not be obvious considering only Clark with Kishi under 35 U.S.C. § 103(a). Accordingly, claim 13 which is dependent on12 is likewise allowable.

The Examiner rejected claim 14 under 35 U.S.C. § 103(a) as being unpatentable in view of Kishi et al. (US597635) in view of Bhawmik (US5680543).

Regarding claim 14 the Examiner indicated that Kishi discloses a device with apparatus that is capable of simultaneously performing self-test on memory circuits and logic circuits including a memory BIST circuit. But actually Kishi teaches a method of where the test is performed when the memory is inactive (during time test) note Kishi Figure2 a. This does not require separate test clock signals to both memory and logic circuits as the clock in the memory circuit is inactive during a retention time test.

The Examiner also indicated that Kishi shows a bypass mode in Figure 6 (selectors 16 through 18). However these are not scan bypass mode operation, instead they switch the memory inputs between the mission mode source (15) and the BIST source (71).

The Examiner did note that Kishi does not disclose generating separate test clock signals to both memory ... logic circuits" but indicates that Bhawmik discloses a clock generator operating related frequencies associated with the scan chains. The Applicant noted that Kishi does not teach or suggest "separate test clock signals"because his solution does not require it since his logic testing takes place at a time when there is no activity at the memory taking advantage of the type of test being performed on the memory being a "a data holding test" requiring no clocking of the memory. Likewise Bhawmik is also solving a different problem and not using separate clock signals which permit in the present invention to clock the memory and the logic at independent frequencies. In fact the Bhawmik teaches a technique where all scan chains are clocked at a given frequency and those scan chains which can not tolerate the magnitude of the frequency are disabled. This would prevent the present invention from testing

simultaneously at two different frequencies. As such Kishi and Bhawmik are teaching away from our invention and it would be impossible to combine such references or to suggest the invention is obvious.

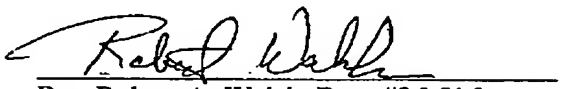
Since Kishmi does not teach or suggest a bypass mode nor using separate clock signals as discussed above and Bhawmik does not teach or suggest a way of generating separate clock signals, it is respectfully submitted that claim 14 is allowable under 35 U.S.C. § 103(a).

**Conclusion**

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,



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